WEST Search History

DATE: Wednesday, December 11, 2002

Set Name side by side	Query	Hit Count	Set Name result set
	DB=USPT; PLUR=YES; OP=ADJ		
L11	L9 and adjust$ near2 (threshold voltage)	9	L11
L10	L9 and threshold voltage	141	L10
L9	L8 and gate and electrode	172	L9
L8	L7 and (wordline or word-line or word line)	354	L8
L7	L6 and sens$	406	L7
L6	L5 and cell	465	L6
L5	L4 and first voltage	472	L5
L4	L3 and second voltage	487	L4
L3	L2 and third voltage	524	L3
L2	L1 and (bitline or bit-line or bit line)	20884	L2
L1	memory and data	301327	L1

END OF SEARCH HISTORY

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Search Results - Record(s) 1 through 9 of 9 returned.

☐ 1. Document ID: US 6452858 B1

L11: Entry 1 of 9 File: USPT Sep 17, 2002

US-PAT-NO: 6452858
DOCUMENT-IDENTIFIER: US 6452858 B1

TITLE: Semiconductor device

DATE-ISSUED: September 17, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Hanzawa; Satoru	Hachioji			JP
Sakata; Takeshi	Kodaira			JP

US-CL-CURRENT: 365/230.06; 365/226, 365/230.01

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

☐ 2. Document ID: US 6418050 B2

L11: Entry 2 of 9 File: USPT Jul 9, 2002

US-PAT-NO: 6418050
DOCUMENT-IDENTIFIER: US 6418050 B2

TITLE: Circuits and methods for a memory cell with a trench plate trench capacitor and a vertical bipolar read device

DATE-ISSUED: July 9, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Forbes; Leonard	Corvallis	OR		

US-CL-CURRENT: 365/177; 365/225.6, 365/230.07

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | Claims | KWIC | Draw Desc | Image

☐ 3. Document ID: US 6411543 B1

L11: Entry 3 of 9 File: USPT Jun 25, 2002

US-PAT-NO: 6411543
DOCUMENT-IDENTIFIER: US 6411543 B1

TITLE: Dynamic random access memory (RAM), semiconductor storage device, and semiconductor integrated circuit (IC) device

DATE-ISSUED: June 25, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Narui; Seiji	Hamura			JP
Nagashima; Osamu	Hamura			JP
Hasegawa; Masatoshi	Ome			JP
Fujisawa; Hiroki	Ome			JP
Miyatake; Shinichi	Ome			JP
Suzuki; Tsuyuki	Akishima			JP
Aoki; Yasunobu	Tachikawa			JP
Takahashi; Tsutom	Tachikawa			JP
Kajigaya; Kazuhiko	Iruma			JP

US-CL-CURRENT: 365/149; 365/226, 365/230.06

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw Desc | Image

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☐ 4. Document ID: US 6201728 B1

L11: Entry 4 of 9 File: USPT Mar 13, 2001

US-PAT-NO: 6201728
DOCUMENT-IDENTIFIER: US 6201728 B1

TITLE: Dynamic RAM, semiconductor storage device, and semiconductor integrated circuit device

DATE-ISSUED: March 13, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Narui; Seiji	Tokyo			JP
Nagashima; Osamu	Tokyo			JP
Hasegawa; Masatoshi	Tokyo			JP
Fujisawa; Hiroki	Tokyo			JP
Miyatake; Shinichi	Tokyo			JP
Suzuki; Tsuyuki	Tokyo			JP
Aoki; Yasunobu	Tokyo			JP
Takahashi; Tsutom	Tokyo			JP
Kajigaya; Kazuhiko	Iruma			JP

US-CL-CURRENT: 365/149; 257/E27.085, 365/226, 365/230.06

5. Document ID: US 6011725 A

L11: Entry 5 of 9 File: USPT Jan 4, 2000

US-PAT-NO: 6011725
DOCUMENT-IDENTIFIER: US 6011725 A

TITLE: Two bit non-volatile electrically erasable and programmable semiconductor memory cell utilizing asymmetrical charge trapping

DATE-ISSUED: January 4, 2000

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Eitan; Boaz	Ra'anana			IL

US-CL-CURRENT: 365/185.33; 257/E29.308, 365/131, 365/185.29

6. Document ID: US 5881014 A

L11: Entry 6 of 9 File: USPT Mar 9, 1999

US-PAT-NO: 5881014
DOCUMENT-IDENTIFIER: US 5881014 A

TITLE: Semiconductor memory device with a voltage down converter stably generating an internal down-converter voltage

DATE-ISSUED: March 9, 1999

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Ooishi; Tsukasa	Hyogo			JP

US-CL-CURRENT: 365/226; 327/536, 365/189.09, 365/227

7. Document ID: US 5781467 A

L11: Entry 7 of 9 File: USPT Jul 14, 1998

US-PAT-NO: 5781467

DOCUMENT-IDENTIFIER: US 57[redacted]67 A

TITLE: Decoding method for ROM matrix having a silicon controlled rectifier structure

DATE-ISSUED: July 14, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Wen; Jemmy	Hsinchu City			TW

US-CL-CURRENT: 365/103; 365/174

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw Desc | Image

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☐ 8. Document ID: US 5742543 A

L11: Entry 8 of 9 File: USPT Apr 21, 1998

US-PAT-NO: 5742543
DOCUMENT-IDENTIFIER: US 5742543 A

TITLE: Flash memory device having a page mode of operation

DATE-ISSUED: April 21, 1998

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Fazio; Albert	Los Gatos	CA		

US-CL-CURRENT: 365/185.21; 365/185.03, 365/185.12, 365/185.13, 365/185.26

Full | Title | Citation | Front | Review | Classification | Date | Reference | Sequences | Attachments | KWIC | Draw Desc | Image

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☐ 9. Document ID: US 5408429 A

L11: Entry 9 of 9 File: USPT Apr 18, 1995

US-PAT-NO: 5408429
DOCUMENT-IDENTIFIER: US 5408429 A

TITLE: Method of altering a non-volatile semiconductor memory device

DATE-ISSUED: April 18, 1995

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Sawada; Kikuzo	Sagamihara			JP

US-CL-CURRENT: 365/185.12; 365/185.18, 365/185.26, 365/185.27, 365/185.33